Remarks

The present amendment responds to the Official Action dated November 23, 2004. The Official Action objected to claim 19 for an improper antecedent. The Official Action rejected claims 14, 15 and 18-23 under 35 U.S.C. §103(a) based on Panwar et al. U.S. Patent No. 5,890,008 (Panwar) in view of Gordon et al. U.S. Patent No. 4,135,247 (Gordon). Claims 16 and 17 were rejected under 35 U.S.C.§103(a) based on Panwar in view of Gordon and further in view of Dowling U.S. Patent No. 6,128,728 (Dowling). Claims 24-27 and 29 were rejected under 35 U.S.C. §103(a) based on Panwar in view of Gordon and further in view of Keckler et al. U.S. Patent No. 5,574,939 (Keckler). Claim 28 was rejected under 35 U.S.C. §103(a) based on Panwar in view of Gordon and Keckler, and further in view of Bapst et al. U.S. Patent No. 6,327,650 (Bapst). These grounds of rejection are addressed below.

Claims 1-13 have been previously cancelled without prejudice. Claims 14, 18, 19, and 21-25 have been amended to be more clear and distinct. In particular, claims 14, 19, and 21-23 have been amended to further clarify the term "physical configuration" to read "physical MxN array organization" or "physical OxP array organization" depending on which array organization applies. Claims 14, 19, and 21-23 have also been amended to add the term "operating configuration." Support for these amendments can be found, for example, in Fig. 3 and its corresponding discussion in the Specification. This amendment is consistent with previously presented claims 21-23 where specific row and column configurations are claimed. Claim 18 has been amended to further clarify the physical identifier of a processing element. Support for this amendment can be found, for example, at page 12, lines 1-19 of the Specification. Claim 19 has

been further amended to correct the antecedent of "the second software task." Claim 24 has been amended to replace the phrase "merged processor configuration" with the phrase "MxN operating configuration" or "OxP operating configuration" in addition to modifications that effectuate this replacement. Claim 24 has been further amended to clarify the specifics of the S/P bit.

Claims 14-29 are presently pending.

Claim 19 Objection

The Examiner now indicates that the antecedent objection made in the Official Action dated July 22, 2004 was improper and thus the implementation of the Examiner's suggestion has now resulted in an improper antecedent for the phrase "a second software task" in line 12. Furthermore the Examiner suggests inserting the term "where" or "wherein" before the phrases "the first software task" in line 9 and "the second software task" in line 12. Claim 19 has been amended to correct the antecedent basis of "the second software task" in line 12 and the term "wherein" has been inserted as the Examiner suggested.

The Art Rejections

As addressed in greater detail below, Panwar, Gordon, Dowling, Keckler and Bapst do not support the Official Action's reading of them and the rejections based thereupon should be reconsidered and withdrawn. Further, the Applicant does not acquiesce in the analysis of

Panwar, Gordon, Dowling, Keckler and Bapst made by the Official Action and respectfully traverses the Official Action's analysis underlying its rejections.

The Official Action repeats the same rejections applied in the Official Action dated July 22, 2004. The Official Action misconstrues the claims and, as a result, fails to meet its burden of showing a prima facia case for obviousness. Due to the Official Action's misconstruction or misunderstanding of the claims as addressed in detail below, the section of Applicant's amendment dated October 7, 2004 addressing the art rejections continues to apply here as well and is incorporated by reference herein. In the interest of conciseness, points made by the Official Action's Response to Argument section will be addressed in order below.

Referring to points 27 and 28 of the Response to Argument section, the Official Action suggests that Panwar's teaching of multiple virtual processors purportedly makes obvious the claimed feature of a physical configuration of at least two processing elements. Applicants respectfully disagree, but in the interest of furthering prosecution offer a claim amendment to further clarify the term "physical configuration." Referring to Fig. 11 of Panwar, Panwar's system of virtual processors which share arithmetic units falls short of the physical configuration expressed in the claims. Referring to Fig. 3 of the present specification, the array processor's physical configuration is expressed in a row and column array organization of the processing elements in order to perform calculations such as matrix operations. When performing matrix operations, for example, each processing element represents a particular element of a matrix. A control status bit (CSB) controls whether the array processor operates in an array configuration

which matches the physical configuration or a compatible operating configuration which corresponds to a different physical configuration.

For example, referring to Figs. 5A and 5B of the present specification, for example, a 1x5 array processor is illustrated where five processing elements, 501, 551, 553, 555, and 557 are specified. This physical configuration of the 1x5 array processor may operate as a 1x5 array processor when a context status bit (CSB) is inactive or a 2x2 array processor when the CSB is active where each processing element executes instructions simultaneously. Specification, page 12, lines 9-15.

As a result, a software task written for an array processor having a different physical configuration advantageously executes on the array processor having the physical configuration. Claim 14, as presently amended, clarifies this advantageous distinction. Claim 14, as presently amended, reads as follows:

> 14. An array processor comprising:
> a physical MxN array organization of at least two processing elements; and
> a processor state register storing a context status bit (CSB), the CSB having a first state and a second state, each processing element operating to detect the state of the CSB,
> the array processor upon detection of the first state of the CSB operating in a first operating context adapted for processing a first software task where the first software task is written for an MxN operating configuration which matches the physical MxN array organization, where M represents the number of rows of processing elements and N represents the number of columns of processing elements,
> the array processor upon detection of the second state of the CSB operating in a second operating context adapted for a second software task where the second software task is written for a second array processor having an OxP operating configuration where O is the number of rows of processing elements and P is the number of columns of processing elements, the OxP operating

configuration not matching the physical MxN array organization as either M≠O, N≠P, or M≠O and N≠P. (emphasis added)

Panwar does not teach and does not suggest "a physical MxN array organization of at least two processing elements ... where M represents the number of rows of processing elements and N represents the number of columns of processing elements." Panwar merely teaches multiple virtual processors which share resources including arithmetic units. Panwar, Fig. 11.

Referring to points 29 and 30 of the Response to Argument section, the Official Action suggests that it would be obvious to store status bits in a status register because Gordon has taught that status bits indicating whether a processor should operate, sleep, nap, or the like may be stored in a register. However, this aspect of Gordon does not meet the feature of the CSB as presently claimed when interpreting claim 14 as a whole. The CSB represents two states. Upon detection of the first state, the operating configuration of the array processor matches the physical configuration of the array processor. Upon detection of the second state, the operating configuration of the array processor is different than the physical configuration of the array processor. Claim 14, as presently amended, recites "the array processor upon detection of the first state of the CSB operating in a first operating context adapted for processing a first software task where the first software task is written for an MxN operating configuration which matches the physical MxN array organization ... the array processor upon detection of the second state of the CSB operating in a second operating context adapted for a second software task where the second software task is written for a second array processor having an OxP operating configuration ... the OxP operating configuration not matching the physical MxN array

organization as either M≠O, N≠P, or M≠O and N≠P." Gordon's status register does not teach and does not suggest tracking the operating configuration as presently claimed in claim 14.

Referring to points 31 and 32 of the Response to Argument section, the Official Action interprets the disclosure at col. 4, lines 15-27 of Panwar as purportedly disclosing that the first software task is written for the physical configuration and that the second software task is written for a second array processor having a different physical configuration. Applicants respectfully disagree, but in the interest of furthering prosecution, claims 14 and 19 have been amended to clarify the phrase "different physical configuration."

Additionally, the Official Action relies on the text of Panwar as teaching or suggesting support of varying different physical configurations when it states "if a first software task has N threads, then there will be a physical configuration of N virtual processing elements, whereas if a second software task has M threads, there will be a physical configuration of M virtual processing elements." Panwar does not disclose a physical relationship between its virtual processing elements. At most, Panwar describes the virtual processors as essentially "merged such that they can share resources efficiently amongst the processors." Panwar, col. 6, lines 56-57.

Referring to points 33 and 34 of the Response to Argument section, the Official Action continues to suggest that virtual processors as taught by Panwar inherently contain physical identifiers. The Official Action relies on Fig. 3 of Panwar as illustrating a physical ID corresponding to the virtual processing element's "physical state." Although the Applicant does not acquiesce in the analysis of this rejection, claim 18 has been amended to further clarify that

the physical identifier results in operating instructions in each processing element according to its physical identifier during the processing of a software task where the operating configuration matches the physical configuration. Claim 18, as presently amended, recites "wherein during the processing of the first software task, instructions are operable in each processing element according to its physical identifier."

Referring to points 35 and 36 of the Response to Argument section, the Official Action again relies on Panwar's virtual processing elements as teaching the SP and PE processors as claimed in claim 24. Claim 24 has been amended to clarify that the merged VLIW SP/PE operates to configure an array processor to operate in an MxN operating configuration or in an OxP operating configuration as described above. Claim 24, as presently amended, reads as follows:

> 24. An apparatus for providing efficient sharing of programming resources in a merged very long instruction word (VLIW) sequence processor (SP) and VLIW processor element (PE) processor, the merged VLIW SP/PE processor operating to configure an array processor to operate in an MxN operating configuration or in an OxP operating configuration, where M and O are the number of rows of processing elements and N and P are the number of columns of processing elements, and where either M≠O or N≠P, the apparatus comprising:
>
> an SP resource file having a first set of registers;
>
> a PE resource file having a second set of registers;
>
> an input for receiving a VLIW presented for execution, the VLIW having at least two instructions, each instruction encoded with a different setting of an SP/PE-bit; and
>
> a processor state register storing a context select bit (CSB), the merged VLIW SP/PE processor reading the values of the CSB and the SP/PE-bit of an instruction to select the MxN operating configuration or the OxP operating configuration when processing the instruction, the MxN operating configuration adapted for accessing at least one register from the second set of registers when processing an SP instruction, the value of the S/P bit determining whether an instruction is executed in the merged VLIW SP/PE processor or is executed in an

array of processing elements defined by the selected operating configuration. (emphasis added)

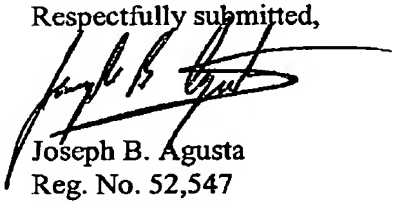
Panwar and Keckler, taken separately or in combination, do not teach and do not suggest different operating configurations of an array processor as claimed in claim 24. In particular, Panwar and Kecler, taken separately or in combination, do not teach and do not suggest selecting an MxN operating configuration or the OxP operating configuration when processing an instruction as presently claimed.

Referring to points 37-40 of the Response to Argument section, these points are moot in light of presently amended claim 24.

Conclusion

All of the presently pending claims, as amended, appearing to define over the applied references, withdrawal of the present rejection and prompt allowance are requested.

Respectfully submitted,



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